

CLAIMS

What is claimed is:

- 5 1. A method for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:
 - accessing a DUT component using an ATE component;
 - performing physical calibration on a first portion of signal pathways coupling the ATE component to the DUT component;
 - 10 performing a simulation based calibration on a second portion of signal pathways coupling the ATE component to the DUT component; and
 - combining physical calibration results with simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.
- 15 2. The method of claim 1, wherein the physical calibration on the first portion of signal pathways is performed using TDT (time domain transfer).
3. The method of claim 1, wherein the simulation based calibration on the second portion of signal pathways is performed using at least one circuit parameterized model of the
20 second portion of the signal pathways.
4. The method of claim 1, wherein the timing propagation delay is calibrated in a signal propagation direction from the ATE component to the DUT component.
- 25 5. The method of claim 1, wherein the timing propagation delay is calibrated in a signal propagation direction from the DUT component to the DUT component.

6. The method of claim 1, wherein the calibration of the timing propagation delay calibrates a pin-to-pin timing skew of the DUT component.

5 7. The method of claim 6, wherein the calibration of the timing propagation delay calibrates DDJ (data depended jitter) of the DUT component.

8. The method of claim 1, further comprising:
performing drive-side calibration using a wide frequency bandwidth wave form and
10 timing measurment means.

9. The method of claim 8, wherein the drive-side calibration is performed at a pogo pin of a loadboard for the DUT component.

15 10. The method of claim 8, wherein the drive-side calibration is performed at a socket mounting pad of a loadboard for the DUT component.

11. The method of claim 1, further comprising:
performing compare-side calibration using a previously calibrated drive-side signal.

20 12. The method of claim 11, wherein the compare-side calibration is performed at a pogo pin or at a socket mounting pad of a loadboard for the DUT component.

13. The method of claim 1, further comprising:
25 moving a deskew calibration point from a pogo pin of a loadboard toward the DUT component.

14. The method of claim 1, further comprising:

moving a deskew calibration point from a socket mounting pad of a loadboard toward the DUT component.

5 15. A system for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:

an ATE component configured for accessing a DUT component, the ATE component configured to perform physical calibration on a first portion of signal pathways coupling the ATE component to the DUT component; and

10 a computer system for performing a simulation based calibration on a second portion of signal pathways coupling the ATE component to the DUT component, wherein physical calibration results are combined with simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.

15 16. The system of claim 15, wherein the physical calibration on the first portion of signal pathways is performed using TDT (time domain transfer).

17. The system of claim 15, wherein the simulation based calibration on the second portion of signal pathways is performed using at least one circuit parameterized model of the
20 second portion of the signal pathways.

18. The system of claim 15, wherein the timing propagation delay is calibrated in a signal propagation direction from the ATE component to the DUT component.

25 19. The system of claim 15, wherein the timing propagation delay is calibrated in a signal propagation direction from the DUT component to the DUT component.

20. The system of claim 15, wherein the calibration of the timing propagation delay calibrates a pin-to-pin timing skew of the DUT component.

21. The system of claim 20, wherein the calibration of the timing propagation delay
5 calibrates DDJ (data depended jitter) of the DUT component.

22. The system of claim 15, further comprising:
performing drive-side calibration using a wide frequency bandwidth waveform and
timing measurement means.

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23. The system of claim 22, wherein the drive-side calibration is performed at a pogo
pin of a loadboard for the DUT component.

24. The system of claim 23, wherein the drive-side calibration is performed at a
15 socket mounting pad of a loadboard for the DUT component.

25. The system of claim 15, further comprising:
performing compare-side calibration using a previously calibrated drive-side signal or
an external pattern generator.

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26. The system of claim 25, wherein the compare-side calibration is performed at a
pogo pin or at a socket mounting pad of a loadboard for the DUT component.

27. The system of claim 15, further comprising:
25 moving a deskew calibration point from a pogo pin of a loadboard toward the DUT
component.

28. The system of claim 15, further comprising:

moving a deskew calibration point from a socket mounting pad of a loadboard toward the DUT component.

5 29. A method for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:

accessing a DUT component using an ATE component;

performing physical calibration on a first portion of signal pathways coupling the ATE component to the DUT component;

10 performing a simulation based calibration on a second portion of signal pathways coupling the ATE component to the DUT component; and

algebraically adding physical calibration results with simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.

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30. A method for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:

accessing a DUT component using an ATE component;

performing a simulation based calibration on signal pathways coupling the ATE

20 component to the DUT component; and

using simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.

31. A method for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:

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accessing a DUT component using an ATE component;

performing physical calibration on a first portion of signal pathways coupling the ATE component to the DUT component, wherein interpolation/extrapolation is used to reduce a number of physical measurements required for covering a plurality of data rates and voltage ranges available to the DUT component;

5 performing a simulation based calibration on a second portion of signal pathways coupling the ATE component to the DUT component; and

combining calibration results with simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.

10 32. A method for improved ATE (automatic test equipment) timing calibration at a DUT (device under test), comprising:

accessing a DUT component using an ATE component;

performing physical calibration on a first portion of signal pathways coupling the ATE component to the DUT component and calibrating signal continuity of the DUT

15 component utilizing signal reflection analysis;

performing a simulation based calibration on a second portion of signal pathways coupling the ATE component to the DUT component; and

combining calibration results with simulation based calibration results to calibrate timing propagation delay between the ATE component and the DUT component.

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